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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/605,254

09/18/2003

Ling-Wuu Yang

9676-US-PA

2253

31561

7590

03/04/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE

7 FLOOR-1, NO. 100

ROOSEVELT ROAD, SECTION 2

TAIPEI, 100

TAIWAN

EXAMINER

KEBEDE, BROOK

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/605,254

**Applicant(s)**

YANG ET AL.

**Examiner**

Brook Kebede

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Drawings*

1. The drawings were received on December 21, 2004. These drawings are not acceptable.

It is respectfully suggested that the drawings change should reflect the figure number of that corresponding to the view number of the sectional view. For example, Fig. 2A is cut out portion of the cross-section taken from Fig. 1A. However, the dotted line along the cross-section of Fig. 1A should be labeled as 2A-2A' or IIA-IIA' not 1-1 or I-I'.

2. The drawings are objected to because of the following reasons:

Figs. 1A – 1G include sectional views I-I'. However, “the ends of the broken line” should be designated by Arabic numerals corresponding to the view number of the sectional view. See 37 C.F.R. § 1.84(h)(3). Additionally, applicant is requested to accordingly amend the specification. For example, see specification in page 4, paragraph [0014], line 4 and throughout.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the

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drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

3. Claim 18 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 18 recites the limitation "The method according to **Claim 18**, further comprising using wet etching to remove the mask layer" in lines 1-2. However, the dependency of claim 18 to itself is improper.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

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invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**5. Claims 1-4, 6-9, 11-14, and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US/6,413,818) in view of Yamauchi (US/5,877,054).**

Re claims 1 and 2, Huang et al. disclose a method of fabricating a flash memory, comprising: sequentially forming a tunneling dielectric layer (303), a first conductive layer (304) and a mask layer (306) on a substrate (300) (see Fig. 3A); patterning the tunneling dielectric layer (303), the first conductive layer (304) and the mask layer (306) to form a plurality of strips (see Fig. 3B); performing an ion implantation step to form a buried drain region (314 315) in the substrate (300) between the strips (see Fig. 3B); forming an insulation (i.e., an isolation oxide) layer (326) between the strips (304 324) (see Fig. 3C); removing the patterned mask layer (306) (see Fig. 3D); etching back the insulation layer (326) to form the insulation layer having a top surface lower than a top surface of the floating gate such that a part of a sidewall of the floating gate is exposed (see Fig. 3G); forming a gate dielectric layer (316) on the top surface and the exposed sidewall of the floating gate; and forming a control gate (360) on the gate dielectric layer (316) (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

However, Huang et al. do not specifically disclose that the top surface of the insulation layer is between a lower and top surface of the patterned conductive layer.

Yamauchi discloses method of fabricating flash memory device the method includes forming of plurality strips comprising a tunnel oxide layer (3), conductive layer (5') and mask layer (8a) (see Fig. 6) having buried source drain regions 2b (see Fig. 7) an insulation layer having the top surface between the tops and the bottom surface of the conductive layer (5')

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between the strips by first forming the conductive layer to cover (fill) the space between the strips and removing the part of the insulation material (4) until the remaining insulation material is between a the top surface and the bottom surface of the conductive layer (5) in order to form a device isolation pattern (see Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

Both Huang et al. and Yamauchi teachings are directed to fabricating of flash memory. The process includes forming of plurality of strips and isolation regions between the strips ~~for~~ for the floating and control gates. Therefore, the teachings of Huang et al. and Yamauchi are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Huang et al. reference with a process forming an insulation layer having the top surface between the tops and the bottom surface of the conductive layer between the strips by first forming the conductive layer to cover (fill) the space between the strips and removing the part of the insulation material until the remaining insulation material is between a the top surface and the bottom surface of the conductive layer as taught by Yamauchi in order to form device isolation between the different device forming active regions.

Re claim 3, as applied to claim 2 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations including the limitation forming the insulation layer with silicon oxide (see Huang et al Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45 and Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

Re claim 4, as applied to claim 2 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations including the limitation using high-density plasma chemical

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vapor deposition for forming the insulation layer (see Huang et al Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45 and Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

Re claim 6, as applied to claim 2 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations including the limitation using CMP or etch back process to remove part of the insulation layer (see Huang et al Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45 and Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

Re claim 7, as applied to claim 2 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations including the limitation using etch back to remove the remaining insulation layer (see Huang et al Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45 and Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

Re claim 8, as applied to claim 1 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations including the limitation forming the mask layer with silicon oxide or silicon nitride (see Huang et al Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45 and Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

Re claim 9, as applied to claim 1 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations including the limitation using wet etching to remove the mask layer (see Huang et al Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45 and Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

Re claims 11 and 12, Huang et al. a method of fabricating a flash memory, comprising: forming a tunneling dielectric layer (303) and a floating gate (304) on a substrate (300); forming a buried drain (315 316) region in the substrate (300) between the floating gates by ion

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implantation step in the substrate between the floating gates (see Fig. 3B); forming an insulation layer on a sidewall of the floating gate (326), the insulation layer having a top surface level between a top surface and a bottom surface of the floating gate (304 324); forming a gate dielectric layer (316) on the top surface and the exposed sidewall of the floating gate; and forming a control gate (360) on the gate dielectric layer (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

However, Huang et al. do not specifically disclose that the top surface of the insulation layer is between a lower and top surface of the patterned floating gate layer.

Yamauchi discloses method of fabricating flash memory device the method includes forming of plurality strips comprising a tunnel oxide layer (3), floating gate layer (5') and mask layer (8a) (see Fig. 6) having buried source drain regions 2b (see Fig. 7) an insulation layer having the top surface between the tops and the bottom surface of the floating gate layer (5') between the strips by first forming the floating gate layer to cover (fill) the space between the strips and removing the part of the insulation material (4) until the remaining insulation material is between a the top surface and the bottom surface of the floating gate layer (5) in order to form a devise isolation pattern (see Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

Both Huang et al. and Yamauchi teachings are directed to fabricating of flash memory the process includes forming of plurality o strips and isolation regions between the strips to for the floating and control gates. Therefore, the teachings of Huang et al. and Yamauchi are analogous.



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Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Huang et al. reference with a process forming an insulation layer having the top surface between the tops and the bottom surface of the floating gate layer between the strips by first forming the floating gate layer to cover (fill) the space between the strips and removing the part of the insulation material until the remaining insulation material is between a the top surface and the bottom surface of the floating gate layer as taught by Yamauchi in order to form device isolation between the different device forming active regions.

Re claim 13, as applied to claim 12 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations including the limitation forming the insulation layer with silicon oxide (see Huang et al Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45 and Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

Re claim 14, as applied to claim 13 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations including the limitation using high-density plasma chemical vapor deposition for forming the insulation layer (see Huang et al Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45 and Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

Re claim 16, as applied to claim 12 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations including the limitation using CMP (see Col. 7, lines 42-46) to remove part of the insulation layer (see Huang et al Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45 and Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

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Re claim 17, as applied to claim 1 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations including the limitation forming a mask on the floating gate when the part of the insulation layer formed subsequently is removed by chemical mechanical polishing; and a step of removing the mask layer before forming the gate dielectric layer, wherein the mask layer is made of a material different from that of the insulation layer (see Huang et al Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45 and Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

Re claim 18, as applied to claim 11 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations including the limitation using wet etching to remove the mask layer (see Huang et al Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45 and Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

Re claim 19, as applied to claim 12 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations including the limitation using etch back to remove the part of the insulation layer (see Huang et al Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45 and Yamauchi Figs. 6-10 and related text in Col. 14, line 1 through Col. 15, line 42).

**6. Claims 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Huang et al. (US/6,413,818) and Yamauchi (US/5,877,054), as applied in Paragraph 5 above, and further in view of Prall (US/5,387,534).**

Re claim 5, as applied to claim 4 in Paragraph 5 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations. However, Hung et al. and Yamauchi do not specifically disclose the using The method TEOS (tetra-ethyl-oxy-silicate) and ozone to from the insulation layer.

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Prall discloses a method of fabrication of a flash memory the method comprises formation of insulation layer (70) using TEOS and ozone in order to provide isolation region between devices (see Figs. 9 and 10; Col. 5, lines 34-41).

Huang et al, Yamauchi and Prall teachings are directed to method of fabricating of flash memory cell device the method includes depositing of an oxide isolation between the floating gates. Therefore, the teachings of Huang et al, Yamauchi and Prall are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Huang et al. and Yamauchi reference with using of TEOS and ozone during formation insulation layer as taught by Prall in order to deposit of an oxide isolation layer that provides isolation between the device regions.

Re claim 15, as applied to claim 14 in Paragraph 5 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations. However, Hung et al. and Yamauchi do not specifically disclose the using The method TEOS (tetra-ethyl-oxy-silicate) and ozone to from the insulation layer.

Prall discloses a method of fabrication of a flash memory the method comprises formation of insulation layer (70) using TEOS and ozone in order to provide isolation region between devices (see Figs. 9 and 10; Col. 5, lines 34-41).

Huang et al, Yamauchi and Prall teachings are directed to method of fabricating of flash memory cell device the method includes depositing of an oxide isolation between the floating gates. Therefore, the teachings of Huang et al, Yamauchi and Prall are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Huang et al. and Yamauchi reference with

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using of TEOS and ozone during formation insulation layer as taught by Prall in order to deposit of an oxide isolation layer that provides isolation between the device regions.

**7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over and Yamauchi (US/5,877,054), as applied in Paragraph 5 above, and further in view of Hsue et al. (US/5,516,713).**

Re claim 10, as applied to claim 4 in Paragraph 5 above, Huang et al. and Yamauchi in combination disclose all the claimed limitations including removing of the silicon nitride mask layer. However, Hung et al. and Yamauchi do not specifically disclose using phosphoric acid as etchant during removal of silicon nitride the mask layer.

Hsue et al. disclose method of fabrication flash memory the method includes depositing of the silicon nitride mask layer (16) and removing of the silicon nitride mask layer using phosphoric acid in order to expose the underlying layer (14) (see Col. 3, lines 13-16).

Huang et al, Yamauchi and Hsue et al. teachings are directed to method of fabricating of flash memory cell device the method includes depositing silicon nitride mask layer and removing of the silicon nitride mask layer in order to expose the underlying layer. Therefore, the teachings Huang et al, Yamauchi and Hsue et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Huang et al. and Yamauchi reference with use phosphoric acid during etching of the silicon nitride layer as taught by Hsue et al. in order to expose the underlying layer.

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***Response to Arguments***

8. Applicants' arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection that was necessitated by the amendment filed on December 21, 2004.

***Conclusion***

9. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Correspondence***


10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK  
February 25, 2005



George Fourson  
Primary Examiner